AMENDMENTS OF THE CLAIMS

This listing of the claims if entered, will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (currently amended) A method of selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, a memory controller, and a plurality of memory modules, each memory module comprising a serial presence detect memory, said method comprising:

counting the number of said memory modules;

keeping a running tally of the number of said memory modules based on said counting;

simultaneously generating multiple clock signals at different frequencies to provide selectable operating speeds of said memory module interface;

determining a maximum speed at which all of the plurality of memory modules can operate;

based on at least a final tally of the number of said memory modules, selecting only one of said multiple clock signals to provide said operating speed of said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selecting, providing said selected clock signal to all of said memory modules.

2. (previously presented) The method of claim 1 wherein said selecting comprises generating memory module interface signals comprising clock, address, and data signals at a frequency based on said final tally of the number of said

memory modules and operating speed information of said memory modules.

3. (previously presented) The method of claim 1 further comprising obtaining information from said serial presence detect memory that includes at least one characteristic of said memory modules, wherein said selecting comprises selecting only one of said multiple clock signals based on at least said final tally of the number of said memory modules and said characteristic.

4. (original) The method of claim 3 wherein said characteristic comprises the number of components in each said memory module.

5. (original) The method of claim 3 wherein said characteristic comprises a speed grade of said memory module.

6. (original) The method of claim 3 wherein said characteristic comprises a manufacturer of said memory module.

7. (original) The method of claim 3 wherein said characteristic comprises a type of said memory module.

8. (original) The method of claim 3 wherein said characteristic comprises a physical layout of signal connections between said memory controller and said memory module.

9. (currently amended) A method of selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, a

memory controller, and a plurality of memory modules, each memory module comprising a serial presence detect memory, said method comprising:

simultaneously generating multiple clock signals at different frequencies to provide selectable operating speeds of said memory module interface;

counting the number of said memory modules;

keeping a running tally of the number of said memory modules based on said counting;

obtaining information from said serial presence detect memory that includes at least one characteristic of said memory module;

determining a maximum speed at which all of the plurality of memory modules can operate;

in accordance with at least a final tally of the number of said memory modules and said obtaining information, selecting only one of said multiple clock signals to provide said operating speed of said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selecting, providing said selected clock signal to all of said memory modules.

10. (original) The method of claim 9 wherein said characteristic comprises a type of said memory module.

11. (currently amended) A method of selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, a memory controller, and a plurality of memory modules, each memory module comprising a serial presence detect memory, said method comprising:

simultaneously generating multiple clock signals at different frequencies to provide selectable operating speeds of said memory module interface;

obtaining information from said serial presence detect memory that includes at least the number of components in each said memory module;

determining a maximum speed at which all of the plurality of memory modules can operate;

in accordance with said obtaining information, selecting only one of said multiple clock signals to provide said operating speed of said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selecting, providing said selected clock signal to all of said memory modules.

12. (currently amended) A method of selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, a memory controller, and a plurality of memory modules, each memory module comprising a serial presence detect memory, said method comprising:

simultaneously generating multiple clock signals at different frequencies to provide selectable operating speeds of said memory module interface;

counting the number of said memory modules;

keeping a running tally of the number of said memory modules based on said counting;

obtaining information from said serial presence detect memory that includes at least a speed grade of said memory module;

determining a maximum speed at which all of the plurality of memory modules can operate;

in accordance with at least a final tally of the number of said memory modules and said obtaining information, selecting only one of said multiple clock signals to provide said operating speed of said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selecting, providing said selected clock signal to all of said memory modules.

13. (currently amended) A computer system comprising:

a central processing unit;

a memory controller including a memory module interface; and

a plurality of memory modules, each memory module including a serial presence detect memory; wherein said memory controller:

simultaneously generates multiple clock signals at different frequencies;

accesses said serial presence detect memory;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

determines a maximum speed at which all of the plurality of memory modules can operate;

based on at least a final tally of the number of said memory modules, selects only one of said multiple clock signals to provide an operating speed of said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selection, provides said selected clock signal to all of said memory modules.

14. (original) The computer system of claim 13 wherein said central processing unit is a microprocessor.

15. (original) The computer system of claim 13 wherein said memory controller obtains information from said serial presence detect memory that includes at least one characteristic of each said memory module.

16. (original) The computer system of claim 15 wherein said characteristic comprises the number of components in each said memory module.

17. (original) The computer system of claim 15 wherein said characteristic comprises a speed grade of said memory module.

18. (original) The computer system of claim 15 wherein said characteristic comprises a manufacturer of said memory module.

19. (original) The computer system of claim 15 wherein said characteristic comprises a type of said memory module.

20. (original) The computer system of claim 15 wherein said characteristic comprises a physical layout of signal connections between said memory controller and said memory module.

21. (currently amended) A computer system comprising:

a central processing unit;

a memory controller including a memory module interface and at least two PLLs to simultaneously generate respective clock signals of different frequencies;

a plurality of memory modules, each memory module including a serial presence detect memory; wherein said memory controller:

accesses said serial presence detect memory;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

obtains information from said serial presence detect memory that includes at least one characteristic of said memory module;

determines a maximum speed at which all of the plurality of memory modules can operate;

based on at least a final tally of the number of said memory modules and said obtained information, selects only one of said clock signals to provide an operating speed of said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selection, provides said selected clock signal to all of said memory modules.

22. (original) The computer system of claim 21 wherein said characteristic comprises the number of components in each said memory module.

23. (currently amended) A computer system comprising:

a central processing unit;

a memory controller including a memory module interface and at least two PLLs to simultaneously generate respective clock signals of different frequencies;

a plurality of memory modules, each memory module including a serial presence detect memory; wherein said memory controller:

accesses said serial presence detect memory;

obtains information from said serial presence detect memory that includes at least the number of components in each memory module;

determines a maximum speed at which all of the plurality of memory modules can operate;

based on at least said obtained information, selects only one of said clock signals to provide an operating speed of said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selection, provides said selected clock signal to all of said memory modules.

24. (currently amended) A computer system comprising:

a central processing unit;

a memory controller including a memory module interface and at least two PLLs to simultaneously generate respective clock signals of different frequencies;

a plurality of memory modules, each memory module including a serial presence detect memory; wherein said memory controller:

accesses said serial presence detect memory;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

obtains information from said serial presence detect memory that includes at least a speed grade of said memory modules or their components;

determines a maximum speed at which all of the plurality of memory modules can operate; and

based on at least a final tally of the number of said memory modules and said obtained information, selects only one of said clock signals to provide an operating speed of said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selection, provides said selected clock signal to all of said memory modules.

25. (currently amended) A computer system comprising:

a central processing unit;

a plurality of memory modules, each memory module including a serial presence detect memory; and

memory controller means including memory module interface means; wherein said memory controller means:

simultaneously generates multiple clock signals at different frequencies;

accesses serial presence detect memory;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

determines a maximum speed at which all of the plurality of memory modules can operate;

based on at least a final tally of the number of said memory modules, selects only one of said multiple clock signals for driving said memory module interface means, wherein said operating speed is slower than the determined maximum speed; and

in response to said selection, provides said selected clock signal to all of said memory modules.

26. (currently amended) A computer system comprising:

a central processing unit;

a plurality of memory modules, each memory module including a serial presence detect memory; and

memory controller means including memory module interface means and means for simultaneously generating multiple clock signals at different frequencies; wherein said memory controller means:

accesses serial presence detect memory;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

obtains information from said serial presence detect memory that includes at least one characteristic of said memory module;

determines a maximum speed at which all of the plurality of memory modules can operate;

based on at least a final tally of the number of said memory modules and said obtained information, selects only one of said multiple clock signals to provide an operating speed of said memory module interface means, wherein said operating speed is slower than the determined maximum speed; and

in response to said selection, provides said selected clock signal to all of said memory modules.

27. (original) The computer system of claim 26 wherein said characteristic comprises a type of said memory module means.

28. (original) The computer system of claim 26 wherein said characteristic comprises a physical layout of signal connections between said memory controller means and said memory module means.

29. (currently amended) A computer system comprising:

a central processing unit;

a plurality of memory modules, each memory module including a serial presence detect memory; and

memory controller means including memory module interface means and means for simultaneously generating multiple clock signals at different frequencies; wherein said memory controller means:

accesses serial presence detect memory;

obtains information from said serial presence detect memory that includes at least the number of components in each memory module means;

determines a maximum speed at which all of the plurality of memory modules can operate;

based on at least said obtained information, selects only one of said multiple clock signals to provide an operating speed of said memory module interface means, wherein said operating speed is slower than the determined maximum speed; and

in response to said selection, provides said selected clock signal to all of said memory modules.

30. (currently amended) A computer system comprising:

a central processing unit;

a plurality of memory modules, each memory module including a serial presence detect memory; and

memory controller means including memory module interface means and means for simultaneously generating multiple clock signals at different frequencies; wherein said memory controller means:

accesses serial presence detect memory;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

obtains information from said serial presence detect memory that includes at least a speed grade of said memory module or its components;

determines a maximum speed at which all of the plurality of memory modules can operate;

based on at least a final tally of the number of said memory modules and said obtained information, selects only one of said multiple clock signals to provide an operating speed of said memory module interface means, wherein said operating speed is slower than the determined maximum speed; and

in response to said selection, provides said selected clock signal to all of said memory modules.

31. (currently amended) A memory controller comprising a memory module interface to a plurality of memory

modules, each memory module including serial presence detect memory; wherein said memory controller:

simultaneously generates multiple clock signals at different frequencies;

accesses serial presence detect memory;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

determines a maximum speed at which all of the plurality of memory modules can operate;

based on at least a final tally of the number of said memory modules, selects only one of said multiple clock signals to provide an operating speed of said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selection, provides said selected clock signal to all of said memory modules.

32. (previously presented) The memory controller of claim 31 wherein said memory controller obtains information from said serial presence detect memory that includes at least one characteristic of said memory module wherein said selected clock signal is also based on said characteristic.

33. (previously presented) The memory controller of claim 32 wherein said characteristic comprises the number of components of said memory module.

34. (previously presented) The memory controller of claim 32 wherein said characteristic comprises a speed grade of said memory module.

35. (previously presented) The memory controller of claim 32 wherein said characteristic comprises a manufacturer of said memory module.

36. (previously presented) The memory controller of claim 32 wherein said characteristic comprises a type of said memory module.

37. (previously presented) The memory controller of claim 32 wherein said characteristic comprises a physical layout of signal connections between said memory controller and said memory module.

38. (currently amended) A memory controller comprising a memory module interface to a plurality of memory modules, each memory module including serial presence detect memory; wherein said memory controller:

simultaneously generates multiple clock signals at different frequencies;

accesses serial presence detect memory;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

obtains information from said serial presence detect memory that includes at least one characteristic of said memory module;

<u>determines a maximum speed at which all of the plurality of memory modules can operate;</u>

based on at least a final tally of the number of said memory modules and said obtained information, selects only one of said multiple clock signals for driving said

memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selection, provides said selected clock signal to all of said memory modules.

39. (original) The memory controller of claim 38 wherein said characteristic comprises a speed grade of said memory module.

40. (currently amended) A memory controller comprising a memory module interface to a plurality of memory modules and at least two PLLs to simultaneously generate respective clock signals of different frequencies, each memory module including serial presence detect memory; wherein said memory controller:

accesses serial presence detect memory;

obtains information from said serial presence detect memory that includes at least the number of components in said memory module;

determines a maximum speed at which all of the plurality of memory modules can operate;

based on said obtained information, selects only one of said clock signals to provide an operating speed of said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selection, provides said selected clock signal to all of said memory modules.

41. (currently amended) A memory controller comprising a memory module interface to a plurality of memory modules, each memory module including serial presence detect memory; wherein said memory controller:

accesses serial presence detect memory;

simultaneously generates multiple clock signals at different frequencies;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

obtains information from said serial presence detect memory wherein said obtained information comprises a speed grade of said memory module;

determines a maximum speed at which all of the plurality of memory modules can operate;

based on at least a final tally of the number of said memory modules and said obtained information, selects only one of said multiple clock signals for driving said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selection, provides said selected clock signal to all of said memory modules.

42. (canceled)

43. (currently amended) Apparatus for selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, a memory controller, and a plurality of memory modules, each memory module comprising a serial presence detect memory, said apparatus comprising:

means for counting the number of said memory modules;

means for keeping a running tally of the number of said memory modules based on said means for counting;

means for determining a maximum speed at which all of the plurality of memory modules can operate;

means for simultaneously generating multiple clock signals at different frequencies to provide selectable operating speeds of said memory interface;

based on at least a final tally of the number of said memory modules, means for selecting only one of said multiple clock signals to provide said operating speed of said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selecting, means for providing said selected clock signal to all of said memory modules.

44. (previously presented) The apparatus of claim 43 wherein said selecting comprises means for generating memory module interface signals comprising clock, address, and data signals at a frequency based on said final tally of the number of said memory modules and operating speed information of said memory modules

45. (previously presented) The apparatus of claim 43 further comprising means for obtaining information from said serial presence detect memory, said information including at least one characteristic of said memory modules; wherein said means for selecting selects one of said multiple clock signals in accordance with at least one of said final tally of the number of said memory modules and said obtained information.

46. (previously presented) The apparatus of claim 45 wherein said characteristic comprises the number of components in each said memory module.

47. (previously presented) The apparatus of claim 45 wherein said characteristic comprises a speed grade of said memory module.

48. (previously presented) The apparatus of claim 45 wherein said characteristic comprises a manufacturer of said memory module.

49. (previously presented) The apparatus of claim 45 wherein said characteristic comprises a type of said memory module.

50. (previously presented) The apparatus of claim 45 wherein said characteristic comprises a physical layout of signal connections between said memory controller and said memory module.

51. (currently amended) Apparatus for selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, a memory controller, and a plurality of memory modules, each memory module comprising a serial presence detect memory, said apparatus comprising:

means for counting the number of said memory modules;

means for keeping a running tally of the number of said memory modules based on said means for counting;

means for simultaneously generating multiple clock signals at different frequencies;

means for obtaining information from said serial presence detect memory that includes at least one characteristic of said memory module;

means for determining a maximum speed at which all of the plurality of memory modules can operate;

in accordance with at least a final tally of the number of said memory modules and obtaining information, means for selecting only one of said multiple clock signals to provide said operating speed of said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selecting, means for providing said selected clock signal to all of said memory modules.

52. (currently amended) Apparatus for selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, a memory controller, and a plurality of memory modules, each memory module comprising a serial presence detect memory, said apparatus comprising:

means for simultaneously generating multiple clock signals at different frequencies;

means for obtaining information from said serial presence detect memory that includes at least the number of components in each said memory module;

means for determining a maximum speed at which all of the plurality of memory modules can operate;

in accordance with at least said means for obtaining information, means for selecting only one of said

multiple clock signals to provide said operating speed of said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selecting, means for providing said selected clock signal to all of said memory modules.

53. (currently amended) Apparatus for selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, and a memory controller, and a plurality of memory modules, each memory module comprising a serial presence detect memory, said apparatus comprising:

means for counting the number of said memory modules;

means for keeping a running tally of the number of said memory modules based on said means for counting;

means for simultaneously generating multiple clock signals at different frequencies;

means for obtaining information from said serial presence detect memory that includes at least a speed grade of said memory module;

means for determining a maximum speed at which all of the plurality of memory modules can operate;

in accordance with at least a final tally of the number of said memory modules and obtaining information, means for selecting only one of said multiple clock signals to provide said operating speed of said memory module interface, wherein said operating speed is slower than the determined maximum speed; and

in response to said selecting, means for providing said selected clock signal to all of said memory modules.